FIG. 1

1

MEMORY 2

CONTROLLER 5

S2

INTEGER ARITHMETIC CONTROLLER SECTION ~21

FINITE FIELD GF (2^m) ARITHMETIC CONTROLLER SECTION ~22

3

4

Z 17Z

Y 17Y

X 17X

R 17R

S1

11~ Y*X∈Z

Y*X∈GF(2m) ~12

13~ SELECTOR

14~ Z+(Y*X)

15

16~ CARRY HOLDER | C+Z+(Y*X)

Y3X0   Y2X0   Y1X0   Y0X0

Y3X1   + ←Y2X1 (+) ←Y1X1 (+) ←Y0X1

29
(Y3X3)   + ←Y2X2 (+) ←Y1X2 (+) ←Y0X2

Y3X3   + ←Y2X3 (+) ←Y1X3 (+) ←Y0X3

0×0

(Y∗X)7   (Y∗X)6   (Y∗X)5   (Y∗X)4   (Y∗X)3   (Y∗X)2   (Y∗X)1   (Y∗X)0

FIG. 2A

Yi Xj

29～ (YiXj)

$(0 \leqq i, j \leqq 3)$

FIG. 2B

IN1

+ ← IN2=EX-OR

OUT

FIG. 2C
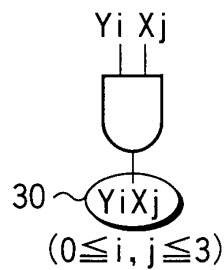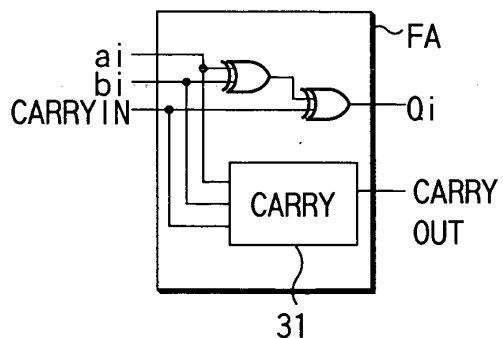
FIG. 3A

FIG. 3B

FIG. 3C

FIG. 3D

FIG. 5

FIG. 6

FIG. 4

FIG. 7

ai
bi
CARRYIN
32
Qi
31
CARRY
33
CARRY-OUT
ctrl (S1)
42

a4
b4
FA
c4
32
θ4
33
a3
b3
FA
c3
32
θ3
33
a2
b2
FA
c2
32
θ2
z3 33
a1
b1
FA
c1
32
θ1
z1
14,15

ai
bi
32
33
CARRYIN
ctrl (S1)
Qi
CARRY
CARRY-OUT
31
43

ai
bi
32
35
34
33'
CARRYIN
1
0 S
Qi
CARRY
CARRY-OUT
31
ctrl (S1)
44

FIG.8

FIG. 9A

FIG. 9B

FIG. 10

FIG. 11

FIG. 12

FIG. 13

FIG. 14

FIG.15

FIG.16

REQUIRED NUMBER OF CLOCKS FOR COMMAND

COMMAND		m=160	m=1024
ADDITION		14	68
MULTIPLY		64	2,116
SQUARE		25	133
DIVIDE	PRE-CALCULATION	35	35
	MAIN BODY	134	2,564

FIG. 17

REQUIRED NUMBER OF CLOCKS FOR $GF(2^{160})$

ARITHMETIC OPERATION	NUMBER OF CLOCKS	SR RATIO
ADDITION	14	ABOUT 4.6 TIMES
MULTIPLY	198	ABOUT 1.2 TIMES
SQUARE	159	ABOUT 1 TIMES

(SR RATIO)=(NUMBER OF CLOCKS)/
            (NUMBER OF CLOCKS IN SHIFT REGISTER CIRCUIT)

FIG. 18

CIRCUIT SIZE (NUMBER OF GATES) OF COPROCESSOR

ARITHMETIC UNIT	8k
CONTROLLER	12.8k
RAM	8.5k
I/F	0.5k
WHOLE	ABOUT 30k

FIG. 19

ADDITIONAL CIRCUIT SIZE (NUMBER OF GATES)
FOR INTEGER BASED COPROCESSOR

ARITHMETIC UNIT	1k
CONTROLLER	3.8k
RAM	0(SHARED)
I/F	0(SHARED)
WHOLE	4.8k

FIG. 20

INDEPENDENT CIRCUIT SIZE (NUMBER OF GATES) OF GF (2^m)

	m=160	m=1024
ARITHMETIC UNIT	3.1k	3.1k
CONTROLLER	3.8k	3.8k
RAM	2.3k	8.5k
I/F	0.5k	0.5k
WHOLE	ABOUT 10k	ABOUT 16k

FIG. 21

FIG. 23

FIG.22

DATA BUS

RAM
EEPROM
ROM

32 BITS

Z' Z | Z3 Z2 Z1 Z0 | Y Y' | Y3 Y2 Y1 Y0 | X | X3 X2 X1 X0 | R | R3 R2 R1 R0 | R'

8 BITS   8 BITS   8 BITS

CONTROL
UNIT FOR
PKC
OPERATIONS
(Commands,
counters,
pointers,
interrupts,
status,
...)

Y*X
(8 BITS * 32 BITS)

40 BITS

Z+(Y*X)
(8 BITS + 40 BITS)

32 BITS

CARRY

C+Z+(Y*X)
(32 BITS+40 BITS)

40 BITS

32 BITS

8 BITS

FIG. 24

INPUT REGISTER

ADDITION

OUTPUT REGISTER

X1

INVERSE
CONTROL

SQUARE

X2

MULTIPLY

81

COPROCESSOR

FIG. 25

FIG.26

FIG.27